

In the Claims:

The following listing replaces all prior versions, and listings of claims in the application.

Listing of Claims:

- 1-18. (Cancelled)
19. (Previously Presented) A patterning method, comprising:
applying an auxiliary layer to a carrier material;
applying a mask layer to the auxiliary layer prior to a production of a cutout;
patterning the mask layer with a lithographic method;
patterning the auxiliary layer and the carrier material with the production of the cutout in accordance with the cutout;
modifying the cutout in a region of the auxiliary layer by isotropic etch-back, where the cutout in a region of the carrier material is not modified or not modified to an extent of the region of the auxiliary layer;
filling the modified cutout with a filling material;
removing the auxiliary layer after filling;
patterning the carrier material using the filling material; and
producing at least one further cutout.
20. (Previously Presented) The method of claim 19, further comprising:
planarizing the filling material prior to patterning the carrier material.
21. (Previously Presented) The method of claim 19, further comprising producing a minimum feature size of less than one hundred nanometers.
22. (Previously Presented) The method of claim 19, further comprising producing a minimum feature size of less than fifty nanometers.
23. (Previously Presented) The method of claim 20, further comprising:
forming a mask layer as a carrier material prior to applying the auxiliary layer; and

patterning a base material using the mask layer after patterning the carrier material using the filling material.

24. (Previously Presented) The method claim 20, further comprising using a semiconductor material as the carrier material.
25. (Previously Presented) The method of claim 24, further comprising forming at least one layer in the expanded cutout prior to filling.
26. (Previously Presented) The method as claimed in claim 25, where forming at least one layer comprises the method of claim 19.
27. (Previously Presented) The method of claim 24, further comprising:
filling the cutout with a further filling material; and
removing the filling material serving for patterning after the filling of the cutout.
28. (Previously Presented) The method of claim 24, further comprising:
partially removing the filling material from the cutout, where one part of a bottom of the cutout is uncovered and another part of a bottom of the cutout remains covered with filling material.
29. (Previously Presented) The method of claim 24, further comprising:
oxidizing the semiconductor material in the region between the cutout and the further cutout.
30. (Withdrawn) A field effect transistor, comprising:
two channel connection regions;
a control region comprising at least two control sections;
an active region that is formed as a projection of a monocrystalline substrate disposed between the channel connection regions and between two control region sections;
insulating regions that are electrically insulating and are disposed between the control region sections and the active region; and
where the projection is isolated from the substrate at a base by an insulating material that is electrically insulating, and where the insulating material ends laterally at the projection in the monocrystalline substrate.

31. (Withdrawn) The field effect transistor of claim 30, where two side areas of the projection that lie at the base of the projection transversely adjoin two substrate areas of the substrate that are disposed in two planes spaced apart from one another by a distance greater than one nanometer.
32. (Withdrawn) The field effect transistor of claim 30, where the control region sections are formed on the two side areas of the projection.
33. (Withdrawn) The field effect transistor of claim 30, where the insulating material does not project beyond at least one side area of the projection.
34. (Previously Presented) The method of claim 19, where modifying the cutout comprises expanding the cutout.
35. (Previously Presented) The method of claim 24, where the carrier material comprises a monocrystalline semiconductor material.
36. (Previously Presented) The method of claim 25, where filling comprises filling with an electrically insulating layer and an electrically conductive layer.
37. (Previously Presented) The method of claim 29, where the region comprises an intermediate region extending from the cutout to the further cutout.
38. (Previously Presented) The method of claim 29, where oxidizing comprises oxidizing prior to the removal of the filling material.
39. (Previously Presented) The method of claim 29, where oxidizing comprises oxidizing after the production of an oxidation protective layer on at least one sidewall of the further cutout.